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EXAMINER	
CHEN, ERIC BRICE	
ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/693,288	LEE, HEON	
	Examiner	Art Unit	
	Eric B. Chen	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *13-19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of claims 1-12 in the reply filed on Oct. 7, 2005 is acknowledged. The traversal is on the grounds that: (1) the newly amended independent claims are no longer limited to dual damascene structures, and therefore could not be manufactured by a materially different process; and (2) the examination of claims 13-19 would not present a serious burden (Applicant's Remarks, pages 8-9).

2. First, the inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case for newly amended claim 1, a magnetic tunnel junction device can be manufactured by forming the spacer layer without anisotropic etching. The sidewalls could be formed by the lift-off technique, rather then etching, or formed by a non-uniform deposition on the stack, such that the film is thicker on the sidewalls of the stack, followed by an isotropic etch. Independent claim 7 remained limited to a dual damascene process.

3. Secondly, burden has been established because the inventions have a separate status in the art as shown by their different classification (Office Action, mailed June 10, 2005, page 2, paragraph 1). Furthermore, burden has been established because the search required for Invention I is not required for Invention II.

4. The requirement is still deemed proper and is therefore made **FINAL**.

Double Patenting

5. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. *See In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

6. A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

7. Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claim Rejections – Double Patenting

8. Claims 2, 6-12 and 20 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 5, 7-11, 15, and 17-20 of copending Application No. 10/692,773, filed Oct. 24, 2003, Lee

("Lee I") (U.S. Patent Appl. Pub. No. 2005/0090111), in view of Chen (U.S. Patent No. 6,627,913). This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

9. As to claim 20, Lee I claims a method of making a magnetic tunnel junction device (Application No. 10/692,773, Applicant's Amendments, filed Sept. 28, 2005, claim 1, lines 5-6), comprising: forming a discrete magnetic tunnel junction stack including a pinned layer (claim 1, lines 17-18); forming an electrically non-conductive spacer layer on the discrete magnetic tunnel junction stack (claim 1, lines 20-21); forming a spacer by anisotropically etching the spacer layer (claim 1, line 23).

10. Lee I further claims forming a magnetic tunnel junction stack (claim 1, line 8); forming a first mask layer on the magnetic tunnel junction stack (claim 1, line 13); patterning the first mask layer (claim 1, line 15); forming a discrete magnetic tunnel junction stack by etching the first mask layer (claim 1, lines 17-18); forming a dielectric layer over the previously fabricated discrete magnetic tunnel junction stack and the spacer (claim 1, lines 25-26); planarizing the dielectric layer to form a substantially planar surface (claim 1, lines 28-30); forming a self-aligned via by etching away a first mask layer (claim 1, line 32); depositing a first electrically conductive material on the dielectric layer and in the self-aligned via (claim 1, lines 34-35); patterning the first electrically conductive material (claim 1, line 36); and forming a dual-damascene conductor by etching the first electrically conductive material (claim 1, lines 38-39).

11. Lee I does not expressly claim forming the spacer layer covering sides of the pinned layer; or the anisotropically-etched spacer covering sides of the pinned layer.

However, Chen discloses a discrete magnetic tunnel junction stack (10) (column 4, lines 14-18; Figure 3) with spacers (50) (column 5, lines 6-7; Figure 5). Chen teaches that magnetic tunnel junction stack (10) includes a pinned layer (column 4, lines 2-13). Chen teaches that the spacers (50) function to alleviate problems with mask misalignment (column 5, lines 49-50), such as overetching along the side of the magnetic tunnel junction stack (column 2, lines 25-30; Figure 2). Moreover, Chen teaches that with the presence of spacer (50) results in greater design tolerances in mask alignment (column 6, lines 14-17, lines 22-24; Figure 2). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the spacer layer covering sides of the pinned layer; or that the anisotropically-etched spacer covers sides of the pinned layer. One who is skilled in the art would be motivated to alleviate problems with mask misalignment.

12. As to claim 2, Lee I claims that the depositing of the first electrically conductive material is continued until the first electrically conductive material completely fills the self-aligned via and the first electrically conductive material extends outward of the substantially planar surface by a predetermined distance (claim 5).

13. As to claim 6, Lee I claims that after the forming of the self-aligned via, the discrete magnetic tunnel junction stack and the self-aligned via are not aligned relative to each other (claim 10).

14. As to claim 7, Lee I claims a method of making a magnetic tunnel junction device from a previously fabricated discrete magnetic tunnel junction stack (claim 11, lines 1-2), comprising: forming an electrically non-conductive spacer layer on the previously

fabricated discrete magnetic tunnel junction stack (claim 11, lines 14-15); forming a spacer by anisotropically etching the spacer layer (claim 11, line 17); forming a dielectric layer over the previously fabricated discrete magnetic tunnel junction stack and the spacer (claim 11, lines 19-20); planarizing the dielectric layer to form a substantially planar surface (claim 11, lines 22-24); forming a self-aligned via by etching away a first mask layer of the previously fabricated discrete magnetic tunnel junction stack (claim 11, line 26); depositing a first electrically conductive material on the dielectric layer and in the self-aligned via (claim 11, lines 28-29); patterning the first electrically conductive material (claim 11, line 31); and forming a dual-damascene conductor by etching the first electrically conductive material (claim 11, lines 33-34).

15. Lee I does not expressly claim that the stack includes free, spacer and pinned layer; the electrically non-conductive spacer layer covers the sides of the free, spacer, and pinned layers; and where the anisotropically-etched spacer covers the sides of the free, spacer and pinned layers. Chen teaches that magnetic tunnel junction stack (10) inherently includes a free, spacer and pinned layer (column 4, lines 2-13). Moreover, Chen discloses a discrete magnetic tunnel junction stack (10) (column 4, lines 14-18; Figure 3) with spacers (50) (column 5, lines 6-7; Figure 5). Chen teaches that the spacers (50) function to alleviate problems with mask misalignment (column 5, lines 49-50), such as overetching along the side of the magnetic tunnel junction stack (column 2, lines 25-30; Figure 2). Moreover, Chen teaches that with the presence of spacer (50) results in greater design tolerances in mask alignment (column 6, lines 14-17, lines 22-24; Figure 2). Therefore, it would have been obvious to one of ordinary skill in the art at

the time the invention was made to form the electrically non-conductive spacer layer covering the sides of the free, spacer, and pinned layers; and where the anisotropically-etched spacer covers the sides of the free, spacer and pinned layers. One who is skilled in the art would be motivated to alleviate problems with mask misalignment.

16. As to claim 8, Lee I claims that the depositing of the first electrically conductive material is continued until the first electrically conductive material completely fills the self-aligned via and the first electrically conductive material extends outward of the substantially planar surface by a predetermined distance (claim 15).

17. As to claim 9, Lee I claims that the spacer layer is conformally deposited on the previously fabricated discrete magnetic tunnel junction stack (claim 17).

18. As to claim 10, Lee I claims that the spacer layer comprises a material selected from the group consisting of silicon oxide and silicon nitride (claim 18).

19. As to claim 11, Lee I claims that the anisotropically etching the spacer layer comprises a reactive ion etch (claim 19).

20. As to claim 12, Lee I claims that after the forming of the self-aligned via, the previously fabricated discrete magnetic tunnel junction stack and the self-aligned via are not aligned relative to each other (claim 20).

Claim Rejections – Double Patenting

21. Claims 2, 6-12 and 20 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-12 of copending Application No. 10/692,612, filed Oct. 24, 2003, Lee ("Lee II") (U.S. Patent

Appl. Pub. No. 2005/0090056), in view of Costrini et al. (U.S. Patent Appl. Pub. No. 2004/0063223), in further view of Chen. This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

22. As to claim 20, Lee II claims a method of making a magnetic tunnel junction device (Applicant's Amendments to the Claims, filed Jan. 31, 2005, claim 1, page 3, lines 6-7), comprising: forming a discrete magnetic tunnel junction stack (claim 1, page 3, line 13-14); forming an electrically non-conductive spacer layer on the discrete magnetic tunnel junction stack (claim 1, page 3, line 16-17); forming a spacer by anisotropically etching the spacer layer (claim 1, page 3, line 19);

23. Lee II claims further claims forming a magnetic tunnel junction stack (page 3, line 9); forming a dielectric layer over the discrete magnetic tunnel junction stack and the spacer (claim 1, page 3, line 21-22); planarizing the dielectric layer to form a substantially planar surface (claim 1, page 3, line 24); forming a self-aligned via by etching (claim 1, page 3, line 28); depositing a first electrically conductive material on the dielectric layer and in the self-aligned via (claim 1, page 3, line 30-31); patterning the first electrically conductive material (claim 1, page 4, line 7); and forming a dual-damascene conductor by etching the first electrically conductive material (claim 1, page 4, line 9).

24. Lee II does not expressly claim forming a first mask layer on the magnetic tunnel junction stack; patterning the first mask layer; forming a discrete magnetic tunnel junction stack by etching the first mask layer; and forming a self-aligned via by etching away the first mask layer. However, Costrini discloses a method of making a magnetic

tunnel junction device (paragraph 0011), including forming a first mask layer (60) (paragraph 0017; Figure 3) on the magnetic tunnel junction stack (100) (Figure 3); patterning the first mask layer (60) (paragraph 0017; Figure 3); forming a discrete magnetic tunnel junction stack by etching the first mask layer (60) (paragraph 0018; Figure 3); and forming a self-aligned via (66) by etching away the first mask layer (60) (paragraph 0023; Figure 6). Moreover, Costrini discloses that forming mask layer (60) enables the formation of a self-aligned vertical electrode to contact the underlying device (paragraph 0013). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the steps of forming a first mask layer on the magnetic tunnel junction stack; patterning the first mask layer; forming a discrete magnetic tunnel junction stack by etching the first mask layer; and forming a self-aligned via by etching away the first mask layer. One who is skilled in the art would be motivated to form an etch mask as part of a process to form a self-aligned vertical electrode to contact the underlying device.

25. Lee II does not expressly claim forming the spacer layer covering sides of the pinned layer; or the anisotropically-etched spacer covering sides of the pinned layer. However, Chen discloses a discrete magnetic tunnel junction stack (10) (column 4, lines 14-18; Figure 3) with spacers (50) (column 5, lines 6-7; Figure 5). Chen teaches that magnetic tunnel junction stack (10) includes a pinned layer (column 4, lines 2-13). Chen teaches that the spacers (50) function to alleviate problems with mask misalignment (column 5, lines 49-50), such as overetching along the side of the magnetic tunnel junction stack (column 2, lines 25-30; Figure 2). Moreover, Chen

teaches that with the presence of spacer (50) results in greater design tolerances in mask alignment (column 6, lines 14-17, lines 22-24; Figure 2). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the spacer layer covering sides of the pinned layer; or that the anisotropically-etched spacer covers sides of the pinned layer. One who is skilled in the art would be motivated to alleviate problems with mask misalignment.

26. As to claim 2, Lee II claims that the depositing of the first electrically conductive material is continued until the first electrically conductive material completely fills the self-aligned via and the first electrically conductive material extends outward of the substantially planar surface by a predetermined distance (claim 2, page 4, lines 11-13).

27. As to claim 6, Lee II claims that after the forming of the self-aligned via, the discrete magnetic tunnel junction stack and the self-aligned via are not aligned relative to each other (claim 6, page 4, lines 25-27).

28. As to claim 7, Lee II claims a method of making a magnetic tunnel junction device from a previously fabricated discrete magnetic tunnel junction stack (claim 7, page 5, lines 1-2), comprising: forming an electrically non-conductive spacer layer on the previously fabricated discrete magnetic tunnel junction stack (claim 7, page 5, lines 4-5); forming a spacer by anisotropically etching the spacer layer (claim 7, page 5, line 7); forming a dielectric layer over the previously fabricated discrete magnetic tunnel junction stack and the spacer (claim 7, page 5, lines 9-10); planarizing the dielectric layer to form a substantially planar surface (claim 7, page 5, line 12); forming a self-aligned via by etching (claim 7, page 5, line 16); depositing a first electrically conductive

material on the dielectric layer and in the self-aligned via (claim 7, page 5, lines 18-19); patterning the first electrically conductive material (claim 7, page 5, line 27); and forming a dual-damascene conductor by etching the first electrically conductive material (claim 7, page 5, line 27).

29. Lee II does not expressly claim forming a self-aligned via by etching away a first mask layer of the previously fabricated discrete magnetic tunnel junction stack. However, Costrini discloses a method of making a magnetic tunnel junction device (paragraph 0011), including forming a self-aligned via (66) by etching away the first mask layer (60) (paragraph 0023; Figure 6) of the previously fabricated discrete magnetic tunnel junction stack. Moreover, Costrini discloses that forming mask layer (60) enables the formation of a self-aligned vertical electrode to contact the underlying device (paragraph 0013). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a self-aligned via by etching away a first mask layer of the previously fabricated discrete magnetic tunnel junction stack. One who is skilled in the art would be motivated to form an etch mask as part of a process to form a self-aligned vertical electrode to contact the underlying device.

30. Lee II does not expressly claim that the stack includes free, spacer and pinned layer; the electrically non-conductive spacer layer covers the sides of the free, spacer, and pinned layers; and where the anisotropically-etched spacer covers the sides of the free, spacer and pinned layers. Chen teaches that magnetic tunnel junction stack (10) inherently includes a free, spacer and pinned layer (column 4, lines 2-13). Moreover, Chen discloses a discrete magnetic tunnel junction stack (10) (column 4, lines 14-18;

Figure 3) with spacers (50) (column 5, lines 6-7; Figure 5). Chen teaches that the spacers (50) function to alleviate problems with mask misalignment (column 5, lines 49-50), such as overetching along the side of the magnetic tunnel junction stack (column 2, lines 25-30; Figure 2). Moreover, Chen teaches that with the presence of spacer (50) results in greater design tolerances in mask alignment (column 6, lines 14-17, lines 22-24; Figure 2). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the electrically non-conductive spacer layer covering the sides of the free, spacer, and pinned layers; and where the anisotropically-etched spacer covers the sides of the free, spacer and pinned layers. One who is skilled in the art would be motivated to alleviate problems with mask misalignment.

31. As to claim 8, Lee II claims that the depositing of the first electrically conductive material is continued until the first electrically conductive material completely fills the self-aligned via and the first electrically conductive material extends outward of the substantially planar surface by a predetermined distance (claim 8, page 6, lines 1-3).

32. As to claim 9, Lee II claims that the spacer layer is conformally deposited on the previously fabricated discrete magnetic tunnel junction stack (claim 9, page 6, lines 5-6).

33. As to claim 10, Lee II claims that the spacer layer comprises a material selected from the group consisting of silicon oxide and silicon nitride (claim 10, page 6, lines 8-10).

34. As to claim 11, Lee II claims that the anisotropically etching the spacer layer comprises a reactive ion etch (claim 11, page 6, lines 12-13).

35. As to claim 12, Lee II claims that after the forming of the self-aligned via, the previously fabricated discrete magnetic tunnel junction stack and the self-aligned via are not aligned relative to each other (claim 12, page 6, lines 15-17)

Claim Rejections - 35 USC § 102

36. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> **A person shall be entitled to a patent unless –**
>
> **(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.**

37. Claims 1 and 3-5 are rejected under 35 U.S.C. 102(e) as being anticipated by Chen (U.S. Patent No. 6,627,913).

38. As to claim 1, Chen discloses a method of making a magnetic tunnel junction device (column 1, lines 5-10), comprising: forming a discrete magnetic tunnel junction stack (10) (column 4, lines 14-18; Figure 3) including a pinned layer (column 4, lines 2-13); forming an electrically non-conductive spacer layer (40) on the discrete magnetic tunnel junction stack (10) (column 4, lines 27-30), the spacer layer (40) covering sides of the pinned layer (Figure 4); forming a spacer (50) by anisotropically etching the spacer layer (40) (column 4, lines 59-61; column 5, lines 6-7), the anisotropically-etched spacer covering sides of the pinned layer (Figure 5). It should be noted that stack (10) includes layers (14), (12), (16), and (30) (column 1, lines 54-65; Figure 3) and a pinned

layer (column 4, lines 2-13). Because spacer layer (40) covers the entire stack (10) (Figure 4), the spacer layer (40) covers the sides of the pinned layer and the anisotropically-etched spacer (50) covers the sides of the pinned layer.

39. As to claim 3, Chen discloses that the spacer layer (40) is conformally deposited on the discrete magnetic tunnel junction stack (10) (column 4, lines 27-29; Figure 4).

40. As to claim 4, Chen discloses that the spacer layer (40) comprises a material selected from the group consisting of silicon oxide and silicon nitride (column 4, lines 29-30).

41. As to claim 5, Chen discloses that the anisotropically etching the spacer layer (40) comprises a reactive ion etch (column 4, lines 59-67).

Claim Rejections - 35 USC § 103

42. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

43. Claims 2, 6-12, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen, in view of Costrini, in further view of Wolf, *Silicon Processing for the VLSI Era*, Vol. 4, Lattice Press (2002).

44. As to claim 7, Chen a method of making a magnetic tunnel junction device (column 1, lines 5-10) from a previously fabricated discrete magnetic tunnel junction stack, the stack including free, spacer and pinned layers (column 1, lines 54-65; Figure

3; column 4, lines 2-13), the method comprising: forming an electrically non-conductive spacer layer (40) on the previously fabricated discrete magnetic tunnel junction stack (10) (column 4, lines 14-18; Figure 3) to cover sides of the free, spacer and pinned layers (column 4, lines 27-29; Figure 4); forming a spacer (50) by anisotropically etching the spacer layer (40) (column 4, lines 59-61; column 5, lines 6-7), where the anisotropically-etched spacer covers the sides of the free, spacer and pinned layers (Figure 5); forming a dielectric layer (70) over the previously fabricated discrete magnetic tunnel junction stack (10) and the spacer (50) (column 5, lines 11-13); planarizing the dielectric layer (70) to form a substantially planar surface (column 5, lines 19-27; Figure 6). It should be noted that stack (10) includes layers (14), (12), (16), and (30) (column 1, lines 54-65; Figure 3) and a pinned layer (column 4, lines 2-13). Because spacer layer (40) covers the entire stack (10) (Figure 4), the spacer layer (40) covers the sides of the pinned layer and the anisotropically-etched spacer (50) covers the sides of the pinned layer. Chen does not expressly disclose the remaining elements, as claimed by the Applicant.

45. Costrini discloses a method of making a magnetic tunnel junction device from a previously fabricated discrete magnetic tunnel junction stack, including forming a self-aligned via (66) by etching away a first mask layer (60) (paragraph 0023; Figure 6) of the previously fabricated discrete magnetic tunnel junction stack; and depositing a first electrically conductive material (92/95) on the dielectric layer (86) and in the self-aligned via (66) (paragraph 0023; Figure 7). Costrini teaches that forming a structure with a first mask layer (60) (paragraph 0023; Figure 6) (or "mandrel") is advantageous because it

enables the formation of a self-aligned vertical electrode (paragraph 0013). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the steps of: forming a self-aligned via by etching away a first mask layer of the previously fabricated discrete magnetic tunnel junction stack; and depositing a first electrically conductive material on the dielectric layer and in the self-aligned via. One who is skilled in the art would be motivated to enable the formation of a self-aligned vertical electrode.

46. Wolf teaches that patterning the first electrically conductive material and forming a dual-damascene conductor by etching the first electrically conductive material are commonly used step in forming the final structure (pages 671-72, Figure 15-1). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the steps of patterning the first electrically conductive material and forming a dual-damascene conductor by etching the first electrically conductive material, because Wolf teaches these steps are commonly used in forming the final device structure.

47. As to claim 8, Costrini discloses that the depositing of the first electrically conductive material (92/95) is continued until the first electrically conductive material completely fills the self-aligned via (66) and the first electrically conductive material (92/95) extends outward of the substantially planar surface by a predetermined distance (paragraphs 0023, 0025; Figure 8).

48. As to claim 9, Chen discloses that the spacer layer (40) is conformally deposited on the discrete magnetic tunnel junction stack (10) (column 4, lines 27-29; Figure 4).

49. As to claim 10, Chen discloses that the spacer layer (40) comprises a material selected from the group consisting of silicon oxide and silicon nitride (column 4, lines 29-30).

50. As to claim 11, Chen discloses that the anisotropically etching the spacer layer (40) comprises a reactive ion etch (column 4, lines 59-67).

51. As to claim 12, Chen does not expressly disclose that after the forming of the self-aligned via, the discrete magnetic tunnel junction stack and the self-aligned via are not aligned relative to each other. However, Chen discloses a discrete magnetic tunnel junction stack (10) (column 4, lines 14-18; Figure 3) with spacers (50) (column 5, lines 6-7; Figure 5). Chen teaches that the spacers (50) function to alleviate problems with mask misalignment (column 5, lines 49-50), such as overetching along the side of the magnetic tunnel junction stack (column 2, lines 25-30; Figure 2). Moreover, Chen teaches that with the presence of spacer (50) results in greater design tolerances in mask alignment (column 6, lines 14-17, lines 22-24; Figure 2). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the self-aligned via, the discrete magnetic tunnel junction stack and the self-aligned via are not aligned relative to each other. One who is skilled in the art would be motivated to adopt a process with greater design tolerances.

52. As to claim 20, Chen discloses that forming the discrete magnetic tunnel junction stack includes forming a magnetic tunnel junction stack (10) (column 4, lines 14-18; Figure 3); forming a dielectric layer (70) over the previously fabricated discrete magnetic tunnel junction stack (10) and the spacer (50) (column 5, lines 11-13); planarizing the

dielectric layer (70) to form a substantially planar surface (column 5, lines 19-27; Figure 6). Chen does not expressly disclose the remaining elements, as claimed by the Applicant.

53. Costrini discloses a method of making a magnetic tunnel junction device from a previously fabricated discrete magnetic tunnel junction stack, including forming a first mask layer (60) (paragraph 0017; Figure 3) on the magnetic tunnel junction stack (100) (Figure 3); patterning the first mask layer (60) (paragraph 0017; Figure 3); forming a discrete magnetic tunnel junction stack by etching the first mask layer (60) (paragraph 0018; Figure 3); forming a self-aligned via (66) by etching away a first mask layer (60) (paragraph 0023; Figure 6) and depositing a first electrically conductive material (92/95) on the dielectric layer (86) and in the self-aligned via (66) (paragraph 0023; Figure 7). Costrini teaches that forming a structure with a first mask layer (60) (paragraph 0023; Figure 6) (or "mandrel") is advantageous because it enables the formation of a self-aligned vertical electrode (paragraph 0013). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the steps of: forming a first mask layer on the magnetic tunnel junction stack; patterning the first mask layer; forming a discrete magnetic tunnel junction stack by etching the first mask layer; forming a self-aligned via by etching away a first mask layer and depositing a first electrically conductive material on the dielectric layer and in the self-aligned via. One who is skilled in the art would be motivated to enable the formation of a self-aligned vertical electrode.

54. Wolf teaches that patterning the first electrically conductive material; and forming a dual-damascene conductor by etching the first electrically conductive material are commonly used step in forming the final structure (pages 671-72, Figure 15-1). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the steps of patterning the first electrically conductive material and forming a dual-damascene conductor by etching the first electrically conductive material, because Wolf teaches these steps are commonly used in forming the final device structure.

55. As to claim 2, Costrini discloses that the depositing of the first electrically conductive material (92/95) is continued until the first electrically conductive material completely fills the self-aligned via (66) and the first electrically conductive material (92/95) extends outward of the substantially planar surface by a predetermined distance (paragraphs 0023, 0025; Figure 8).

56. As to claim 6, Chen does not expressly disclose that after the forming of the self-aligned via, the discrete magnetic tunnel junction stack and the self-aligned via are not aligned relative to each other. However, Chen discloses a discrete magnetic tunnel junction stack (10) (column 4, lines 14-18; Figure 3) with spacers (50) (column 5, lines 6-7; Figure 5). Chen teaches that the spacers (50) function to alleviate problems with mask misalignment (column 5, lines 49-50), such as overetching along the side of the magnetic tunnel junction stack (column 2, lines 25-30; Figure 2). Moreover, Chen teaches that with the presence of spacer (50) results in greater design tolerances in mask alignment (column 6, lines 14-17, lines 22-24; Figure 2). Therefore, it would have

been obvious to one of ordinary skill in the art at the time the invention was made to form the self-aligned via, the discrete magnetic tunnel junction stack and the self-aligned via are not aligned relative to each other. One who is skilled in the art would be motivated to adopt a process with greater design tolerances.

Response to Arguments

57. Applicant's arguments (Applicant' Remarks, pages 7-8), filed Oct. 7, 2005, with respect to the rejection of claims 1-12 as either anticipated by, or obvious in view of Costrini have been fully considered and are persuasive. Applicant has pointed out that the Costrini reference does not teach a spacer layer covering sides of the pinned layer (page 7). Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Chen.

58. Applicant's arguments (Applicant' Remarks, page 8), filed Oct. 7, 2005, with respect to the rejection of claims 1-12 under the judicially-created doctrine of double patenting have been fully considered and are persuasive. Applicant has pointed out that the Lee I and Lee II references does not claim a spacer layer covering sides of the pinned layer (page 7). However, upon further consideration, a new ground(s) of rejection is made in view of Chen.

Conclusion

59. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric B. Chen whose telephone number is (571) 272-2947. The examiner can normally be reached on Monday through Friday, 8AM to 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine G. Norton can be reached on (571) 272-1465. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EBC EBC
Nov. 22, 2005

SHAMIM AHMED
PRIMARY EXAMINER